Patent Claims

1. A vertical nano-transistor
with a source region (S),
with a drain region (D),
with a gate region (G) and
with a semiconductor channel region (3) between the source region (S) and the drain region (D),
the gate region (G) being formed by a metal film (1) in which the transistor is embedded such that the gate region (G) and the semiconductor channel region (3) form a coaxial structure and the source region (S), the semiconductor channel region (3) and the drain region (D) are arranged in a vertical direction and
the gate region (G) is provided with an electrical insulation (2) against the source region (S), the drain region (D) and the semiconductor channel region (3).

2. The transistor of claim 1,
in which the semiconductor channel region (3) is structured cylindrically.

3. The transistor of claim 1,
in which the thickness of the metal film (1) forming the vertical gate region (G) is less than 100 µm, preferably 5 to 20 µm.

4. The transistor of claim 1,
in which the diameter of the semiconductor channel region (3) is several ten to several hundred nanometers.

5. The transistor of claim 1,
in which the thickness of the electrical insulation (2) between the gate region (G) and the semiconductor channel (3) is several ten to several hundred

nanometers.

6. The transistor of claim 1,
in which the thickness of the insulation layer (2) on the upper and lower surface of the metal film (1) is several micrometers.

7. The transistor of claim 1,
wherein the material of the semiconductor channel (3) is CuSCN or TiO_2 or PbS or ZnO or another compound semiconductor.

8. The transistor of claim 1,
wherein the material for the source (S) and the drain (D) region is Au or Ag or Cu or Ni or Al.

9. The transistor of claim 1,
wherein the source (S) and the drain (D) region are structured as dots.

10. A memory arrangement,
in which a plurality of vertical nano-transistors is arranged according to at least one of the preceding claims adjacent each other in a metal film.

11. A method of fabricating vertical nano-transistors according to claim 1, including at least the following method steps
- forming holes (4) in a thin metal film (1) constituting the gate region (G) of the transistor, for forming the channel region (3),
- applying insulation material to the walls of the holes (4),
- applying insulation material to the upper and lower surface of the metal film (1),
- applying semiconductor material in the insulated holes (4) for forming the semiconductor channel region (3),
- applying contacts for forming the source (S) and drain (D) regions.

12. The method of claim 11,

wherein the holes (4) in the metal film (1) are formed by focused ion beams.

13. The method of claim 11,

wherein the holes (4) in the metal film (1) are formed by a laser beam.

14. The method of claim 11,

wherein the insulation material is applied to the upper and lower surface of the metal film (1) by thin-film technology.

15. The method of claim 11,

wherein the insulation material is applied to the wall of the holes (4) and to the upper and lower surface of the metal foil (1) by vacuum filtration of a polymer solution.

16. The method of claim 11,

wherein the insulation material is applied to the wall of the holes (4) and to the upper and lower surface of the metal foil (1) by electro-chemical deposition.

17. The method of claim 11,

wherein the insulation material is applied to the wall of the holes (4) and to the upper and lower surface of the metal foil (1) by chemical deposition.

18. The method of claim 11,

wherein the material used for the semiconductor channel region (3) is CuSCN or TiO_2 or PbS or ZnO or another compound semiconductor.

19. The method of claim 11,

wherein the semiconductor material is introduced into the insulated holes (4) by electro-chemical bath precipitation.

20. The method of claim 11,

wherein the semiconductor material is introduced into the insulated holes (4) by chemical deposition.

21. The method of claim 11,

wherein the semiconductor material is introduced into the insulated holes (4) by the ILGAR process.

22. The method of claim 11,

wherein the material used for the source and drain region is Au or Ag or Cu or Ni or Al.